AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently Amended) An integrated circuit ~~for point-to-point simultaneous bidirectional differential high speed signalling to another integrated circuit connected thereto, the integrated circuit~~ comprising:

a transmitter ~~for transmitting~~to transmit a first signal to another integrated circuit, wherein the transmitter ~~having~~ has a transmitter buffer having a transmitter buffer output and a transmitter buffer input;

a receiver ~~for receiving~~to receive a second signal from the other integrated circuit, wherein the receiver ~~having~~ has a receiver buffer ~~and co-located on the same integrated circuit~~having a receiver buffer output and a receiver buffer input, the receiver buffer input coupled to the transmitter buffer output; and

a differential buffer coupled between the transmitter buffer input ~~of the transmitter buffer~~ and the ~~output of the~~ receiver buffer output,

~~wherein the first signal at the output of the transmitter buffer is coupled into the input of the receiver buffer co-located on the same integrated circuit;~~

~~wherein a third signal at the input of the transmitter buffer is passed through the differential buffer and coupled onto the output of the receiver buffer;~~

wherein the differential buffer is configured to accept a third signal from the input of the transmit buffer and to adjust~~s~~ the third signal in phase and amplitude to cancel the first signal at the output of the receiver buffer~~, whereby the quality of receiving the second signal is enhanced by canceling echoing of the first signal~~.

2. (Original) The integrated circuit according to claim 1, wherein the third signal is further adjusted in rise time.

3. (Currently Amended) The integrated circuit according to claim 1, wherein the gain and phase characteristics of the differential buffer ~~is~~ are varied by means of a finite state machine using a training pattern following either power up or ~~on~~ a request.

4. (Currently Amended) The integrated circuit according to claim ~~1~~3, wherein the differential buffer is implemented as a chain of buffer stages.

5. (Currently Amended) The integrated circuit according to claim ~~1~~4, further comprising one or more digital to analog converters coupled between the finite state machine and the differential buffer, a peak detector coupled between the finite state machine and the output of the receiver, and wherein the finite state machine is configured to vary the gain and phase characteristics of the differential buffer by reading~~employs a peak detector and means of reading~~ a parameter from~~related to~~ the peak detector, via the analog-to-digital converters, and to set a value ~~through~~ on the digital to analogue converters ~~which~~ to control~~s~~ ~~the~~ one or more variable current~~s~~ sources in the ~~differential stages in the~~ chain of buffer~~s~~ stages based at least in part on the read parameter~~providing the third signal between the transmitter and receiver~~.

6. (Currently Amended) The integrated circuit according to claim 1, wherein the differential buffer has a variable current source ~~for the purpose of~~ to allow ~~setting~~control ~~the~~ of amplitude or phase characteristics of the ~~third signal~~differential buffer.

7. (Currently Amended) The integrated circuit according to claim 1, further comprising a finite state machine to set a programmable or variable load ~~wherein~~ of the differential buffer ~~has a programmable or variable load which is set by a finite state machine following a training pattern initiated after power-up or on request.~~to allow control of amplitude or phase characteristics of the differential buffer.

8. (Currently Amended) The integrated circuit according to claim 1, wherein the differential buffer includes a coarse delay circuit, a fine delay circuit, an amplitude control circuit, and a rise-time control circuit and wherein the integrated circuit further comprises ~~controlled by~~ a finite state machine to control the coarse delay circuit, the fine delay circuit, the amplitude control circuit, and the rise-time control circuit to vary phase and amplitude characteristics of the differential buffer to adjust the third signal in phase and amplitude to cancel ~~the~~a first signal echo component of the second signal at the output of the receiver buffer.

9. (Currently Amended) The integrated circuit according to claim 8, wherein the ~~output amplitude, phase and rise time of the differential buffer~~ finite state machine is configured to vary the phase and amplitude characteristics of the differential buffer as part of a calibration

procedure ~~-is varied by means of a finite state machine using a training pattern~~ following either power up or a request.

10. (Canceled)

11. (Currently Amended) The integrated circuit according to claim 8, wherein the coarse delay circuit comprises a digital delay line, a pair of multiplexers, and logic ~~for~~ to control ~~of~~ the multiplexers.

12. (Currently Amended) The integrated circuit according to claim ~~9~~11, wherein the digital delay line comprises a cascade of buffers.

13. (Currently Amended) The integrated circuit according to claim ~~9~~11, further ~~wherein~~ comprising a pair of multiplexers configured to select~~s~~ signals from the digital delay line.

14. (Currently Amended) The integrated circuit according to claim 9, wherein ~~a~~ the finite state machine is configured to generate~~s~~ control signals to select ~~the~~ signals from the digital delay line in the coarse delay circuit to vary~~ing~~ the delay of the third signal through the differential buffer~~with respect to the first signal~~.

15. (Canceled)

16. (Canceled)

17. (Currently Amended) The integrated circuit according to claim 1, ~~wherein~~ further comprising a finite state machine ~~plus~~ and an analog-to-digital converter ~~(ADC)~~ to ~~generates~~provide ~~the~~ a control voltage to the differential buffer to vary the amplitude of the third signal.

18. (Original) The integrated circuit according to claim 8, wherein the amplitude control circuit comprises a buffer with a variable load.

19. (Currently Amended) The integrated circuit according to claim 18, wherein the finite state machine is configured to control a gate voltage of an NMOS transistor to vary the variable load ~~comprises a NMOS transistor whose gate voltage and therefore resistance is controlled by the finite state machine~~.

20. (Currently Amended) The integrated circuit according to claim ~~9~~8, wherein the rise-time control circuit comprises switches, capacitors, and control logic.

21. (Currently Amended) The integrated circuit according to claim 9, wherein ~~a~~ the finite state machine is configured to generate~~s~~ control signals to ~~switch the capacitors in~~ the rise-time control circuit ~~varying~~ to vary the rise-time of the third signal.

22. (Currently Amended) The integrated circuit according to claim ~~16~~5, wherein the peak detector comprises an amplitude cancellation sensor, a phase cancellation sensor, and an analog~~ue~~ multiplexer.

23. (Currently Amended) The integrated circuit according to claim [[4]]22, wherein the finite state machine is configured to adjust ~~controls the~~ another amplitude and/or another phase ~~adjustment~~ characteristic of the other integrated circuit ~~on power-up or on request, sequentially, first the master and then the slave~~during a calibration phase.

24. (Currently Amended) The integrated circuit according to claim ~~23~~22, wherein the amplitude cancellation sensor comprises an integrator ~~plus~~ and a sample and hold device.

25. (Currently Amended) The integrated circuit according to claim ~~24~~22, wherein ~~the timing of the phases for~~ the ~~integrator~~phase cancellation sensor is configured to cycle through ~~includes~~ a reset phase, an integration phase, and a transfer phase during a calibration phase.

26. (Currently Amended) The integrated circuit according to claim 25, wherein the finite state machine is configured to control the timing of the phases~~for the phase sensor is controlled by the finite state machine~~.

27. (Currently Amended) The integrated circuit according to claim ~~1~~22, wherein the finite state machine is further configured to inject patterns ~~are injected~~ into the transmitter ~~for the purpose of~~ and to measure ~~measuring the~~ a resulting offset in the amplitude cancellation sensor.

28. (Currently Amended) The integrated circuit according to claim 22, wherein the phase cancellation sensor comprises a full-wave rectifier plus integrator and a sample and hold circuit.

29. (Currently Amended) The integrated circuit according to claim 24, wherein the integrator ~~includes~~ is configured to cycle through a reset phase, an integration phase, and a transfer phase.

30. (Currently Amended) The integrated circuit according to claim 28, wherein the finite state machine is further configured to control the timing of the phases for the phase cancellation sensor ~~is controlled by the finite state machine~~.

31. (Canceled).

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Currently Amended) A method ~~for echo cancellation in simultaneous bidirectional differential high speed signalling, where the signalling is from one integrated circuit connected to another integrated circuit, each circuit comprising a transmitter having an output buffer and a receiver having a receiver buffer, the method~~ comprising:

transmitting a first signal from ~~the~~ an output buffer of ~~the~~ a transmitter arranged on ~~one~~ an integrated circuit, to another integrated circuit, the first signal also being coupled ~~also~~ into ~~the~~ an input buffer of ~~the~~ a receiver ~~co-located with the transmitter~~arranged on the ~~same~~ integrated circuit;

receiving a second signal from the other integrated circuit;

transmitting a third signal from the input of the transmitter buffer through a differential buffer;

~~where~~ adjusting, by the differential buffer, the third signal ~~is adjusted~~ in phase and amplitude; and

coupling the adjusted third signal onto the output of ~~the receiving~~ an output buffer of the receiver to cancel ~~the~~ a first signal echo component of the second signal~~, whereby the quality of receiving the third signal is enhanced by canceling echoing of the first signal~~.

36. (Currently Amended) A method according to claim 35, wherein ~~the~~ a phase of the third signal ~~applied to the output of the receiving buffer~~ is opposite to ~~the~~ a phase of the first signal.

37. (Currently Amended) A method according to claim 35, wherein ~~the~~ a third rise time of the third signal ~~applied to the output of the receiving buffer~~ is adjusted to match ~~the~~ a first rise time of the first signal.

38. (Currently Amended) A method according to claim 35 wherein ~~the~~ a gain property of the differential buffer is varied at least in part by ~~means of a finite state machine~~ using a training pattern.

39. (Currently Amended) A method according to claim 35 wherein adjusting the phase and/or amplitude of the third signal ~~is adjusted by~~comprises:

applying a training pattern ~~and minimising~~ to an input of the transmitter~~,~~;

varying a digital-to-analog code applied to a digital-to-analog converter ~~(DAC)~~ to adjust operating parameters of the differential buffer~~,~~;

measuring resulting noise conditions corresponding to each applied digital-to-analog code; ~~using a peak detector and ADC to~~

determin~~e~~ing ~~which~~ a digital-to-analog code that corresponds to ~~the~~ a minimum noise condition~~,~~; and

~~using state machine and~~ applying the determined digital-to-analog code to the ~~DACs~~ ~~D~~digital-to-~~A~~analog ~~C~~converter ~~at the end of adjustment process~~to calibrate the differential buffer.

40. (Canceled)